

WHAT IS CLAIMED IS:

1 1. A hardware queue circuit for managing a plurality of linked lists
2 comprising:
3 a head of queue (HOQ) memory to store information representative of a head
4 entry associated with each of the linked lists;
5 a tail of queue (TOQ) memory to store information representative of a tail
6 entry of each of the linked lists;
7 a data memory to store data associated with entries of the linked lists;
8 a next pointer memory;
9 an address bus configured to selectively deliver information the HOQ memory
10 and from the TOQ memory to the data memory in order to access a memory location in the
11 data memory and to the next pointer memory in order to access a memory location in the next
12 pointer memory;
13 a free pointer memory;
14 a first data bus configured to deliver data from an accessed memory location
15 in the next point memory to the free pointer memory and to the HOQ memory; and
16 a second data bus configured to deliver data from an accessed memory
17 location in the free pointer memory to an accessed memory location in the next pointer
18 memory.

1 2. The circuit of claim 1 wherein the HOQ memory comprises N first
2 registers and the TOQ memory comprises N second registers.

1 3. The circuit of claim 1 further comprising a link length memory to store
2 information representative of a length of each of the linked lists.

1 4. The circuit of claim 1 further comprising a controller component
2 configured to effect a write operation of first data to a first linked list by operating the circuit
3 to perform method steps of:

4 obtaining a first value stored in a location in the TOQ memory that is
5 associated with the first linked list;
6 storing the first data in a location in the data memory that is determined from
7 the first value;
8 obtaining a second value stored in the free pointer memory;

9 storing the second value in a memory location of the next pointer memory that
10 is determined from the first value; and

11 storing the second value in the location in the TOQ memory that is associated
12 with the first linked list.

1 5. The circuit of claim 4 wherein the TOQ memory comprises a plurality
2 of registers, wherein the first linked list is associated with one of the registers.

1 6. The circuit of claim 5 wherein the free pointer memory is organized as
2 a queue and the step of obtaining the second value includes performing a pop operation on
3 the free pointer memory.

1 7. The circuit of claim 1 further comprising a controller component
2 configured to effect a read operation on a first linked list by operating the circuit to perform
3 method steps of:

4 obtaining a first value stored in a location in the HOQ memory that is
5 associated with the first linked list;

6 reading data stored in a location in the data memory that is determined from
7 the first value;

8 obtaining a second value stored in a memory location of the next pointer
9 memory that is determined from the first value;

10 storing the first value in the free pointer memory; and

11 storing the second value in the location in the HOQ memory that is associated
12 with the first linked list.

1 8. The circuit of claim 7 wherein the HOQ memory comprises a plurality
2 of registers, wherein the first linked list is associated with one of the registers.

1 9. A method for operating hardware to access one or more linked lists
2 comprising:

3 accessing a first memory to obtain first queue data representative of a first
4 linked list, the first memory configured to store a plurality of queue data representative of a
5 plurality of linked lists, the first queue data representing at least one entry in the first linked
6 list;

7 accessing a first location in a second memory based on first address
8 information contained in the first queue data, wherein data associated with the at least one
9 entry can be written to the first location or read from the first location;
10 accessing a third memory to obtain second address information representative
11 of a second location in the second memory, the second location in the second memory for
12 storing data associated with a next entry in the first linked list;
13 storing either the first address information or the second address information
14 in a fourth memory, depending on whether data is written to the first location or data is read
15 from the first location; and
16 associating the second address information with the first queue data.

1 10. The method of claim 9 wherein the first, second, third, and fourth
2 memories, each is a memory component separate from the others.

1 11. The method of claim 9 wherein the first memory is a register file
2 comprising a plurality of first registers and a plurality of second registers,
3 each first register associated with a linked list, each first register storing a first
4 location in the second memory, the first location for storing data associated with an entry that
5 represents the beginning of a linked list,
6 each second register associated with a linked list, each second register storing
7 a second location in the second memory, the second location for storing data associated with
8 an entry that represents the end of a linked list.

1 12. The method of claim 11 wherein the register file further comprises a
2 plurality of third registers, each third register associated with a linked list, each third register
3 storing a value indicative of the number of entries contained in its associated linked list.

1 13. The method of claim 9 wherein, when data is written to the first
2 location, the third memory contains information representative of one or more addresses
3 which represent available locations in the second memory for storing data, the fourth memory
4 stores information which indicates an order in which data associated with a linked list is
5 stored in the second memory, the second address information is a location in the second
6 memory for storing data associated with a subsequent write operation to the first linked list,
7 and the step of storing is a step of storing the second address information in the fourth
8 memory.

1 14. The method of claim 13 further comprising determining if there is
2 sufficient memory in the second memory when data is written to the first location.

1 15. The method of claim 13 further comprising incrementing a counter
2 associated with the first linked list when data is written to the first location.

1 16. The method of claim 9 wherein, when data is read from the first
2 location in the second memory, the third memory stores information which indicates an order
3 in which data associated with a linked list is stored in the second memory, the fourth memory
4 contains information representative of one or more addresses which represent available
5 locations in the second memory for storing data, the second address information is a location
6 in the second memory from which data will be read in response to a subsequent read
7 operation on the first linked list, and step of storing is a step of storing the first address
8 information in the fourth memory thereby making the first location available for storing data.

1 17. The method of claim 16 further comprising decrementing a counter
2 associated with the first linked list when data is read from the first location.

1 18. Apparatus for accessing one or more linked lists comprising:
2 a first memory for storing a plurality of queue data representative of a plurality
3 of linked lists;
4 a second memory;
5 a third memory for storing link address information representative of an
6 ordering of data in the second memory that are associated with a linked list;
7 a fourth memory for storing free address information representative of
8 unallocated memory locations in the second memory;
9 means for accessing the first memory to obtain first queue data representative
10 of a first linked list, the first queue data representing at least one entry in the first linked list
11 means for accessing a first location in the second memory based on first
12 address information contained in the first queue data, wherein data associated with the at least
13 one entry can be written to the first location or read from the first location;
14 means, responsive to a write operation, for:
15 accessing the fourth memory to obtain second address information
16 representative of a second location in the second memory;
17 storing the second address information in the third memory; and

18 storing the second address information in the first queue data,
19 wherein data associated with a subsequent write operation will be
20 stored the second location;
21 means, responsive to a read operation, for:
22 accessing the third memory to obtain third address information
23 representative of a second location in the second memory;
24 storing the first address information in the fourth memory; and
25 storing the third address information in the first queue data,
26 wherein a subsequent read operation will be made from the third
27 location.

1 19. The apparatus of claim 18 wherein the first, second, third, and fourth
2 memories, each is a memory component separate from the others.

1 20. The apparatus of claim 18 wherein the first memory is a register file
2 comprising a plurality of first registers and a plurality of second registers,
3 each first register associated with a linked list, each first register storing a first
4 location in the second memory, the first location for storing data associated with an entry that
5 represents the beginning of a linked list,
6 each second register associated with a linked list, each second register storing
7 a second location in the second memory, the second location for storing data associated with
8 an entry that represents the end of a linked list.